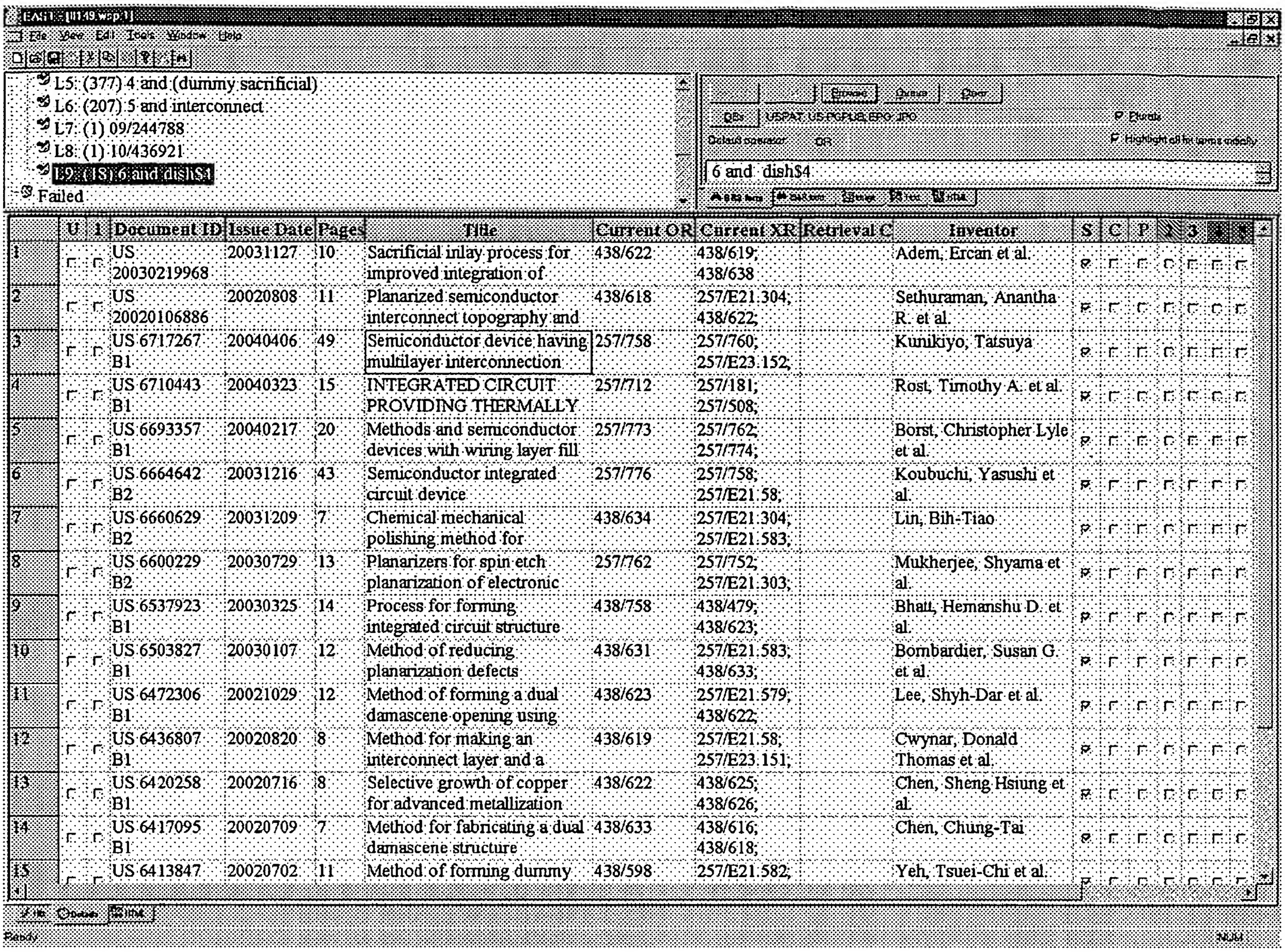

	U	I	Document ID	Issue Date	Pages	Title	Current OR	Current XR	Retrieval C	Inventor	S	C	P	2	3	4	5
1	☐	☐	US 20030219968	20031127	10	Sacrificial inlay process for improved integration of	438/622	438/619; 438/638		Adem, Ercan et al.	☑	☐	☐	☐	☐	☐	☐
2	☐	☐	US 20020106886	20020808	11	Planarized semiconductor interconnect topography and	438/618	257/E21.304; 438/622;		Sethuraman, Anantha R. et al.	☑	☐	☐	☐	☐	☐	☐
3	☐	☐	US 6717267 B1	20040406	49	Semiconductor device having multilayer interconnection	257/758	257/760; 257/E23.152;		Kunikiyo, Tatsuya	☑	☐	☐	☐	☐	☐	☐
4	☐	☐	US 6710443 B1	20040323	15	INTEGRATED CIRCUIT PROVIDING THERMALLY	257/712	257/181; 257/508;		Rost, Timothy A. et al.	☑	☐	☐	☐	☐	☐	☐
5	☐	☐	US 6693357 B1	20040217	20	Methods and semiconductor devices with wiring layer fill	257/773	257/762; 257/774;		Borst, Christopher Lyle et al.	☑	☐	☐	☐	☐	☐	☐
6	☐	☐	US 6664642 B2	20031216	43	Semiconductor integrated circuit device	257/776	257/758; 257/E21.58;		Koubuchi, Yasushi et al.	☑	☐	☐	☐	☐	☐	☐
7	☐	☐	US 6660629 B2	20031209	7	Chemical mechanical polishing method for	438/634	257/E21.304; 257/E21.583;		Lin, Bih-Tiao	☑	☐	☐	☐	☐	☐	☐
8	☐	☐	US 6600229 B2	20030729	13	Planarizers for spin etch planarization of electronic	257/762	257/752; 257/E21.303;		Mukherjee, Shyama et al.	☑	☐	☐	☐	☐	☐	☐
9	☐	☐	US 6537923 B1	20030325	14	Process for forming integrated circuit structure	438/758	438/479; 438/623;		Bhatt, Hemanshu D. et al.	☑	☐	☐	☐	☐	☐	☐
10	☐	☐	US 6503827 B1	20030107	12	Method of reducing planarization defects	438/631	257/E21.583; 438/633;		Bombardier, Susan G. et al.	☑	☐	☐	☐	☐	☐	☐
11	☐	☐	US 6472306 B1	20021029	12	Method of forming a dual damascene opening using	438/623	257/E21.579; 438/622;		Lee, Shyh-Dar et al.	☑	☐	☐	☐	☐	☐	☐
12	☐	☐	US 6436807 B1	20020820	8	Method for making an interconnect layer and a	438/619	257/E21.58; 257/E23.151;		Cwynar, Donald Thomas et al.	☑	☐	☐	☐	☐	☐	☐
13	☐	☐	US 6420258 B1	20020716	8	Selective growth of copper for advanced metallization	438/622	438/625; 438/626;		Chen, Sheng Hsiung et al.	☑	☐	☐	☐	☐	☐	☐
14	☐	☐	US 6417095 B1	20020709	7	Method for fabricating a dual damascene structure	438/633	438/616; 438/618;		Chen, Chung-Tai	☑	☐	☐	☐	☐	☐	☐
15	☐	☐	US 6413847	20020702	11	Method of forming dummy	438/598	257/E21.582;		Yeh, Tsuei-Chi et al.	☑	☐	☐	☐	☐	☐	☐